

# CX3SM CRYSTAL

800 kHz to 1.35 MHz

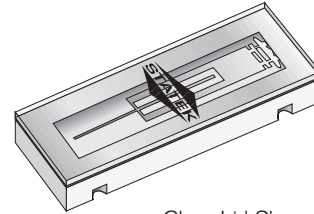
Low Profile Miniature Surface Mount Quartz Crystal

## DESCRIPTION

The CX3SM quartz crystals are leadless devices designed for surface mounting on printed circuit boards or hybrid substrates. They are hermetically sealed in a rugged, miniature ceramic packages and are designed specifically for manufacturing temperatures up to 260°C.

## FEATURES

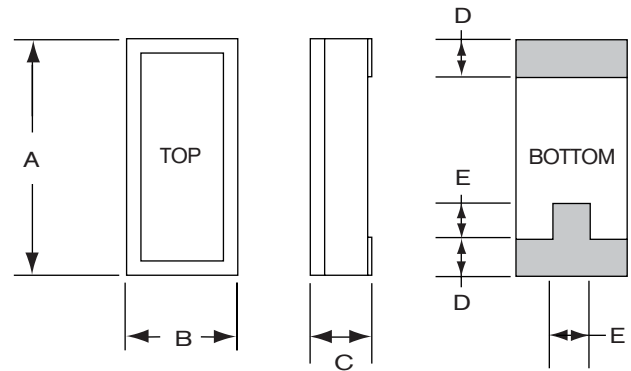
- Extensional mode
- Ideal for use with microprocessors
- Designed for low power applications
- Compatible with hybrid or PC board packaging
- Low aging
- Full military testing available
- Ideal for battery operated applications
- Designed and manufactured in the USA



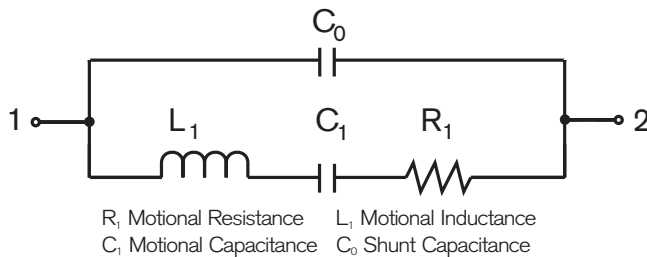
Glass Lid Shown

actual size  
side view

## PACKAGE DIMENSIONS



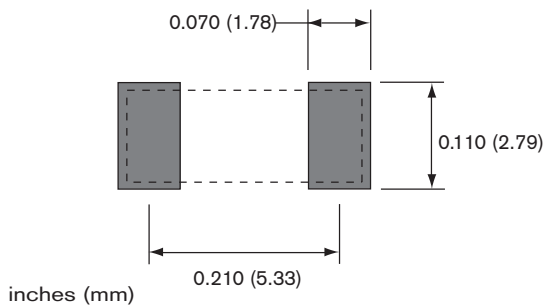
## EQUIVALENT CIRCUIT



DIM	TYP.		MAX.	
	inches	mm	inches	mm
A	0.263	6.68	0.270	6.86
B	0.097	2.46	0.104	2.64
C	-	-	see below	
D	0.052	1.32	0.058	1.47
E	0.030	0.76	0.035	0.89

DIM "C"	GLASS LID		CERAMIC LID	
	inches	mm	inches	mm
MAX				
SM1	0.053	1.35	0.067	1.70
SM2	0.055	1.40	0.069	1.75
SM3	0.058	1.47	0.072	1.83

## SUGGESTED LAND PATTERN



## SPECIFICATIONS

Specifications are typical at 25°C unless otherwise noted. Specifications are subject to change without notice.

Frequency Range	800 kHz - 1.35 MHz
Functional Mode	Extensional
Calibration Tolerance*	± 500 ppm (0.05%) ± 1000 ppm (0.1%) ± 10000 ppm (1.0%)
Load Capacitance	7 pF
Motional Resistance (R <sub>1</sub> )	5 kΩ MAX
Motional Capacitance (C <sub>1</sub> )	1.2 fF
Quality Factor (Q)	150 k
Shunt Capacitance (C <sub>0</sub> )	1.0 pF
Drive Level	3 μW MAX.
Turning Point (T <sub>0</sub> )**	35°C
Temperature Coefficient (k)	-0.035 ppm/°C <sup>2</sup>

Note: Frequency f at temperature T is related to frequency f<sub>0</sub> at turning point temperature T<sub>0</sub> by:  $\frac{f-f_0}{f_0} = k(T-T_0)^2$

Aging, first year	5 ppm MAX
Shock, survival	1000 g peak, 0.3 ms, 1/2 sine
Vibration, survival	10 g RMS, 20-1,000 Hz random
Operating Temp. Range	-10°C to +70°C (Commercial) -40°C to +85°C (Industrial) -55°C to +125°C (Military)
Storage Temp. Range	-55°C to +125°C
Max Process Temperature	260°C for 20 sec.

\* Tighter tolerances available.  
\*\* Other values available.

## PACKAGING OPTIONS

CX3SM	- Tray Pack
	- Tape and Reel
	(Reference tape and reel data sheet 10109)

## TERMINATIONS

Designation	Termination
SM1	Gold Plated
SM2	Solder Plated
SM3	Solder Dipped

## HOW TO ORDER CX3SM CRYSTALS

CX3	S	C	SM1	-	1.0M <sub>k</sub>	/	M
"S" if special or custom design. Blank if Std.	SM1 = Gold Plated SM2 = Solder Plated SM3 = Solder Dipped	Blank = Glass Lid C = Ceramic Lid	Calibration Tolerance @ 25°C (in ppm)	Frequency K = kHz M = MHz	Operating Temp. Range: C = -10°C to +70°C I = -40°C to +85°C M = -55°C to +125°C S = Customer Specified		

## TYPICAL APPLICATION FOR A PIERCE OSCILLATOR

The low profile CX miniature surface mount crystal is ideal for small, high density, battery operated portable products. The CX crystal designed in a Pierce oscillator (single inverter) circuit provides very low current consumption and high stability. A conventional CMOS Pierce oscillator circuit is shown below. The crystal is effectively inductive and in a PI-network circuit with C<sub>D</sub> and C<sub>G</sub> provides the additional phase shift necessary to sustain oscillation. The oscillation frequency (f<sub>0</sub>) is 15 to 150 ppm above the crystal's series resonant frequency (f<sub>S</sub>).

### Drive Level

R<sub>A</sub> is used to limit the crystal's drive level by forming a voltage divider between R<sub>A</sub> and C<sub>D</sub>. R<sub>A</sub> also stabilizes the oscillator against changes in the amplifiers output resistance (R<sub>O</sub>). R<sub>A</sub> should be increased for higher voltage operation.

### Load Capacitance

The CX crystal calibration tolerance is influenced by the effective circuit capacitances, specified as the load capacitance (C<sub>L</sub>). C<sub>L</sub> is approximately equal to:

$$C_L = \frac{C_D \times C_G}{C_D + C_G} + C_S \quad (1)$$

NOTE: C<sub>D</sub> and C<sub>G</sub> include stray layout to ground and C<sub>S</sub> is the stray shunt capacitance between the crystal terminal. In practice, the effective value of C<sub>L</sub> will be less than that calculated from C<sub>D</sub>, C<sub>G</sub> and C<sub>S</sub> values because of the effect of the amplifier output resistance. C<sub>S</sub> should be minimized.

The oscillation frequency (f<sub>0</sub>) is approximately equal to:

$$f_0 = f_S \left[ 1 + \frac{C_1}{2(C_0 + C_L)} \right] \quad (2)$$

Where  
f<sub>S</sub> = Series resonant frequency of the crystal  
C<sub>1</sub> = Motional Capacitance  
C<sub>0</sub> = Shunt Capacitance

## CONVENTIONAL CMOS PIERCE OSCILLATOR CIRCUIT

